What is claimed is:

1. A unit pixel for use in a complementary metal oxide semiconductor (CMOS) image sensor, comprising:

a photodiode formed in a predetermined location of an active area;

a transfer transistor disposed between the photodiode and a floating diffusion node, wherein a transfer control signal is applied to a gate;

a reset transistor disposed between the photodiode and a power supply voltage (VDD) terminal, wherein a reset control signal is applied to a gate and a VDD is applied to a drain;

a drive transistor of which a drain is connected to the VDD terminal and a gate is connected to the floating diffusion node;

a selection transistor of which a drain is connected to a source of the drive transistor and a source is connected to an output terminal, wherein a selection control signal is applied to a gate; and

a dummy transistor disposed between the drive transistor and the floating diffusion node, of which a gate is connected to the floating diffusion node.

2. The unit pixel as recited in claim 1, wherein the dummy transistor has a threshold voltage higher than an operation voltage so that the dummy transistor keeps to be turned off.

3. The unit pixel as recited in claim 2, wherein the dummy transistor has a high threshold voltage region which is overlapped portions of the floating diffusion node and the gate of the dummy transistor.

4. The unit pixel as recited in claim 3, wherein the high threshold voltage region is formed by means of boron (B^{11}) ions implantation on condition that an ion implantation energy ranges from about 20 keV to about 40 keV and a dose amount ranges from about 1.0×10^{12} atoms/㎠ to about 9.0×10^{13} atoms/㎠.

5. The unit pixel as recited in claim 3, wherein the high threshold voltage region is formed by means of BF_2 ions implantation on condition that an ion implantation energy ranges from about 40 keV to about 60 keV and a dose amount ranges from about 1.0×10^{12} atoms/㎠ to about 9.0×10^{13} atoms/㎠.

6. The unit pixel as recited in claim 1, wherein the gate of the drive transistor and the gate of the dummy transistor are formed as a single gate of a conductive material.

7. The unit pixel as recited in claim 1, wherein the gate of the drive transistor is electrically connected to the floating diffusion node through a butting contact.

8. The unit pixel as recited in claim 7, wherein the butting contact employs a tungsten.

9. The unit pixel as recited in claim 1, wherein the gate of the drive transistor is electrically connected to the floating diffusion node through a bridge interconnection.

10. The unit pixel as recited in claim 9, wherein the bridge connection uses a salicide.

11. The unit pixel as recited in claim 1, wherein the active area includes:

a first active area where the photodiode is formed; and

a second active area having a loop shape that each end is connected to a side of the first active area.

12. The unit pixel as recited in claim 11, wherein the second active area has:

a first region extended from one corner of the side of the photodiode, where the transfer transistor and the floating diffusion node are formed;

a second region formed perpendicular to the first region, where the drive transistor, the dummy transistor and the selection transistor are formed; and

a third region formed perpendicular to the second region where the VDD terminal and the reset transistor are formed, wherein one end of the third region is connected to the other

corner of the side of the photodiode.

13. The unit pixel as recited in claim 12, wherein the second region is contained a conductive well.

14. The unit pixel as recited in claim 12, wherein the gate of the drive transistor includes:

a first drive gate region which is parallel with the second region separated by a predetermined distance;

a second drive gate region formed perpendicular to the first drive gate region, wherein a portion of the second drive gate region is overlapped the second region; and

a third drive gate region formed perpendicular to the first region separated from the second drive gate region by a predetermined distance, the third drive gate region serving as the gate of the dummy transistor.

15. A CMOS image sensor having a plurality of unit pixels, said each unit pixel comprising:

a photodiode formed in a predetermined location of an active area;

a transfer transistor disposed between the photodiode and a floating diffusion node, wherein a transfer control signal is applied to a gate;

a reset transistor disposed between the photodiode and a power supply voltage (VDD) terminal, wherein a reset control signal is applied to a gate and a VDD is applied to a drain;

a drive transistor of which a drain is connected to the VDD terminal and a gate is connected to the floating diffusion node;

a selection transistor of which a drain is connected to a source of the drive transistor and a source is connected to an output terminal, wherein a selection control signal is applied to a gate; and

a dummy transistor disposed between the drive transistor and the floating diffusion node, of which a gate is connected to the floating diffusion node.

16. The CMOS image sensor as recited in claim 15, wherein the dummy transistor has a threshold voltage higher than an operation voltage so that the dummy transistor keeps to be turned off.

17. The CMOS image sensor as recited in claim 16, wherein the dummy transistor has a threshold voltage region which is overlapped a portion of the floating diffusion node and the gate of the dummy transistor.

18. The unit pixel as recited in claim 17, wherein the high threshold voltage region is formed by means of boron (B^{11}) ions implantation on condition that an ion implantation energy ranges from about 20 keV to about 40 keV and a dose amount ranges from about 1.0×10^{12} atoms/㎠ to about 9.0×10^{13} atoms/㎠.

19. The unit pixel as recited in claim 17, wherein the high threshold voltage region is formed by means of BF_2 ions implantation on condition that an ion implantation energy ranges from about 40 keV to about 60 keV and a dose amount ranges from about 1.0×10^{12} atoms/㎠ to about 9.0×10^{13} atoms/㎠.

20. The CMOS image sensor as recited in claim 15, wherein the gate of the drive transistor and the gate of the dummy transistor are formed as a single gate of a conductive material.

21. The CMOS image sensor as recited in claim 15, wherein the gate of the drive transistor is electrically connected to the floating diffusion node through a butting contact.

22. The CMOS image sensor as recited in claim 15, wherein the gate of the drive transistor is electrically connected to the floating diffusion node through a bridge interconnection.

23. The CMOS image sensor as recited in claim 22, wherein the bridge connection uses a salicide.